

What is claimed is:

1 1. An active matrix display device having a display
2 region consisting of sub-pixels arrayed in a matrix fashion,
3 the sub-pixels having switching elements, comprising:
4 a plurality of data and scan signal lines, and common
5 voltage lines for sending signals and a reference
6 voltage to the sub-pixels;
7 first test transistors, each of which is connected to
8 one of the plurality of scan signal lines for
9 sending first test signals thereto; and
10 a plurality of first input terminals, each of which is
11 connected to one of a plurality of the first test
12 transistors;
13 wherein each gate of the first test transistors and
14 each of the common voltage lines are connected to
15 one of the first input terminals, the first test
16 transistors control inputs of the first test
17 signals to the sub-pixels.

1 2. The device as claimed in claim 1, wherein each of
2 the sub-pixels comprises:
3 a switching transistor having a gate coupled to one of
4 the scan signal lines, a drain/source coupled to
5 one of the data signal lines; and
6 a storage capacitor coupled between one of the common
7 voltage lines and a source/drain of the switching
8 transistor.

1 3. The device as claimed in claim 1 further
2 comprising:

3 a data driver generating the data signals; and
4 a scan driver generating the scan signals.

1 4. The device as claimed in claim 1 further
2 comprising:

3 second test transistors, each of which is connected to
4 one of the plurality of the data signal lines for
5 sending second test signals thereto; and
6 a plurality of second input terminals, each of the
7 second input terminals is connected to one of a
8 plurality of the second test transistors;
9 wherein each gate of the second test transistors and
10 each of the common voltage lines are connected to
11 one of the second input terminals, the second
12 test transistors control inputs of the second
13 test signals to the sub-pixels.

1 5. A liquid crystal display panel comprising:

2 an array substrate on which an active matrix display
3 device is formed, wherein the active matrix
4 display device comprises:

5 a plurality of data and scan signal lines, and
6 common voltage lines for sending signals and
7 a reference voltage to the sub-pixels;
8 test transistors, each of which is connected to
9 one of the plurality of scan signal lines
10 for sending test signals thereto; and

11 a plurality of input terminals, each of which is
12 connected to one of a plurality of the test
13 transistors;
14 wherein each gate of the test transistors and each
15 of the common voltage lines are connected to
16 one of the input terminals, the test
17 transistors control inputs of the test
18 signals to the sub-pixels;
19 a facing substrate having a common electrode; and
20 a liquid crystal sealed between the array and facing
21 substrate.

1 6. The panel as claimed in claim 5, wherein each of
2 the sub-pixels further comprises:

3 a switching transistor having a gate coupled to one of
4 the scan signal lines, a drain/source coupled to
5 one of the data signal lines; and
6 a storage capacitor coupled between one of the common
7 voltage lines and a source/drain of the switching
8 transistor.

1 7. The panel as claimed in claim 5, wherein the
2 active matrix display device further comprises:

3 a data driver generating the data signals; and
4 a scan driver generating the scan signals.

1 8. An active matrix display device having a display
2 region consisting of sub-pixels arrayed in a matrix fashion,
3 the sub-pixels having switching elements, comprising:

4 a plurality of data and scan signal lines, and common
5 voltage lines for sending signals and a reference
6 voltage to the sub-pixels;
7 test transistors, each of which is connected to one of
8 the plurality of scan signal lines for sending
9 test signals thereto; and
10 a plurality of input terminals, each of which is
11 connected to one of a plurality of the test
12 transistors;
13 wherein each gate of the test transistors and each of
14 the common voltage lines are connected to one of
15 the input terminals, the test transistors control
16 inputs of the test signals to the sub-pixels, the
17 display region is composed of a plurality of
18 blocks, the scan signal lines included in a first
19 block of the plurality of blocks are connected to
20 a first set of the input terminals via
21 sources/drains of the test transistors, and the
22 scan signal lines included in a second block of
23 the plurality of blocks are connected to a second
24 set of the input terminals different from the
25 first set of the input terminals via the
26 sources/drains of the test transistors.

1 9. An active matrix display device comprising:
2 an array substrate having sub pixel sections arrayed in
3 a matrix fashion, each sub pixel section having a
4 switching element, the array substrate including:

5 a plurality of data signal lines and a plurality
6 of scan signal lines for sending signals to
7 the sub pixel sections;
8 test transistors, each of which is connected to
9 one of the plurality of scan signal lines
10 for sending test signals thereto; and
11 a plurality of input terminals for inputting the
12 test signals;
13 wherein drains or sources of the test transistors are
14 connected to the scan signal lines, gates of a
15 plurality of the test transistors and the common
16 voltage lines are connected to a first input
17 terminal of the plurality of input terminals, the
18 sources or drains of a plurality of the test
19 transistors are connected to a second input
20 terminal of the plurality of input terminals, and
21 the test transistors control inputting of the
22 test signals to the sub pixel sections.

1 10. The active matrix display device as claimed in
2 claim 9, wherein the switching elements of the sub pixel
3 sections and the test transistors are thin film transistors
4 formed of amorphous silicon.

1 11. The active matrix display device as claimed in
2 claim 9, wherein the sources or drains of the test
3 transistors that are connected to adjacent ones of the data
4 signal lines are connected to different ones of the
5 plurality of input terminals.

1 12. The active matrix display device as claimed in
2 claim 9, wherein the sources or drains of the test
3 transistors that are connected to adjacent ones of the scan
4 signal lines are connected to different ones of the
5 plurality of input terminals.

1 13. The active matrix display device as claimed in
2 claim 9, wherein the gates of all of the test transistors
3 connected to the scan signal lines on the array substrate
4 are connected to the first input terminal.

1 14. The active matrix display device as claimed in
2 claim 9, further comprising: a drive circuit connected to
3 the plurality of data signal lines and the plurality of scan
4 signal lines, wherein when the drive circuit controls
5 inputting of a screen display signal, all of the test
6 transistors are held in an OFF state.

1 15. The active matrix display device as claimed in
2 claim 9, further comprising an opposing substrate opposite
3 to the array substrate.

1 16. An active matrix display device having a display
2 region consisting of sub-pixels arrayed in a matrix fashion,
3 the sub-pixels having switching elements, comprising:

4 a plurality of data and scan signal lines, and common
5 voltage lines for sending signals and a reference
6 voltage to the sub-pixels;
7 first test transistors, each of which is connected to
8 one of the plurality of scan signal lines for
9 sending first test signals thereto;

10 second test transistors, each of which is connected to
11 one of the plurality of data signal lines for
12 sending second test signals thereto; and
13 a plurality of first and second input terminals, each
14 of the first input terminals is connected to one
15 of a plurality of the first test transistors and
16 each of the second input terminals is connected
17 to one of a plurality of the second test
18 transistors;
19 wherein each gate of the first test transistors and
20 each of the common voltage lines are connected to
21 one of the first input terminals, each gate of
22 the second test transistors and each of the
23 common voltage lines are connected to one of the
24 second input terminals, the first and second test
25 transistors control inputs of the first and
26 second test signals to the sub-pixels.

1 17. An active matrix display device having a display
2 region consisting of sub-pixels arrayed in a matrix fashion,
3 the sub-pixels having switching elements, comprising:
4 a plurality of data and scan signal lines, and common
5 voltage lines for sending signals and a reference
6 voltage to the sub-pixels;
7 test transistors, each of which is connected to one of
8 the plurality of data signal lines for sending
9 test signals thereto; and
10 a plurality of input terminals, each of which is
11 connected to one of a plurality of the test
12 transistors;

13 wherein each gate of the test transistors and each of
14 the common voltage lines are connected to one of
15 the input terminals, the test transistors control
16 inputs of the test signals to the sub-pixels.

1 18. A method for driving an active matrix display
2 device having a display region consisting of sub-pixels
3 arrayed in a matrix fashion, the sub-pixels having switching
4 elements, the method comprising the steps of:

5 sending signals and a reference voltage to the sub-
6 pixels through a plurality of data and scan
7 signal lines, and common voltage lines;
8 sending first test signals to one of the plurality of
9 scan signal lines through test transistors; and
10 sending second test signals to gates of the test
11 transistors;
12 wherein the second test signals are used as the
13 reference voltage sent to the pixel through the
14 common voltage lines when the test transistors
15 are turned off by the second test signals.

1 19. A display circuit comprising:
2 a pixel array having pixels each of said pixels coupled
3 to a first, a second and a third line to receive
4 a scan signal, a data signal and a common voltage
5 respectively; and
6 a plurality of transistors having drains/sources
7 coupled to the first lines, sources/drains
8 coupled to receive first signals and gates
9 commonly coupled to receive a second signal;

10 wherein the transistors are turned on by the second
11 signal so that the first signals are transmitted
12 on the first lines to drive the pixels during a
13 test, and the transistors are turned off by the
14 second signal so that the first signals are
15 isolated from the first lines and the second
16 signal is used as the common voltage supplied to
17 the pixels through the third lines beyond the
18 test.

1 20. The circuit as claimed in claim 19, wherein each
2 of the pixels comprises:

3 a second transistor having a gate coupled to one of the
4 first lines, a drain/source coupled to the second
5 line; and
6 a storage capacitor coupled between one of the third
7 lines and a source/drain of the second
8 transistor.

1 21. The circuit as claimed in claim 19 further
2 comprising:

3 a data driver generating the data signals; and
4 a scan driver generating the scan signals.

1 22. A liquid crystal display panel comprising:
2 an array substrate on an LCD circuit is formed, wherein
3 the LCD circuit comprises:
4 a pixel array having pixels each of said pixels
5 coupled to a first, a second and a third
6 line to receive a scan signal, a data signal

7 and a common voltage respectively, and each
8 of the pixels has a pixel electrode; and
9 a plurality of transistors having drains/sources
10 coupled to the first lines, sources/drains
11 coupled to receive a first signal and gates
12 coupled to receive a second signal;
13 wherein the transistors are turned on by the
14 second signal so that the first signals are
15 transmitted on the first lines to drive the
16 pixels during a test, and the transistors
17 are turned off by the second signal so that
18 the first signals are isolated from the
19 first lines and the second signal is used as
20 the common voltage supplied to the pixels
21 through the third lines beyond the test;
22 a facing substrate having a common electrode; and
23 a liquid crystal sealed between the array and facing
24 substrate.

1 23. The panel as claimed in claim 22, wherein each of
2 the pixels further comprises:

3 a second transistor having a gate coupled to one of the
4 first lines, a drain/source coupled to the second
5 line; and
6 a storage capacitor coupled between one of the third
7 lines and a source/drain of the second
8 transistor.

1 24. The panel as claimed in claim 22, wherein the LCD
2 circuit further comprises:

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3 a data driver generating the data signals; and
4 a scan driver generating the scan signals.